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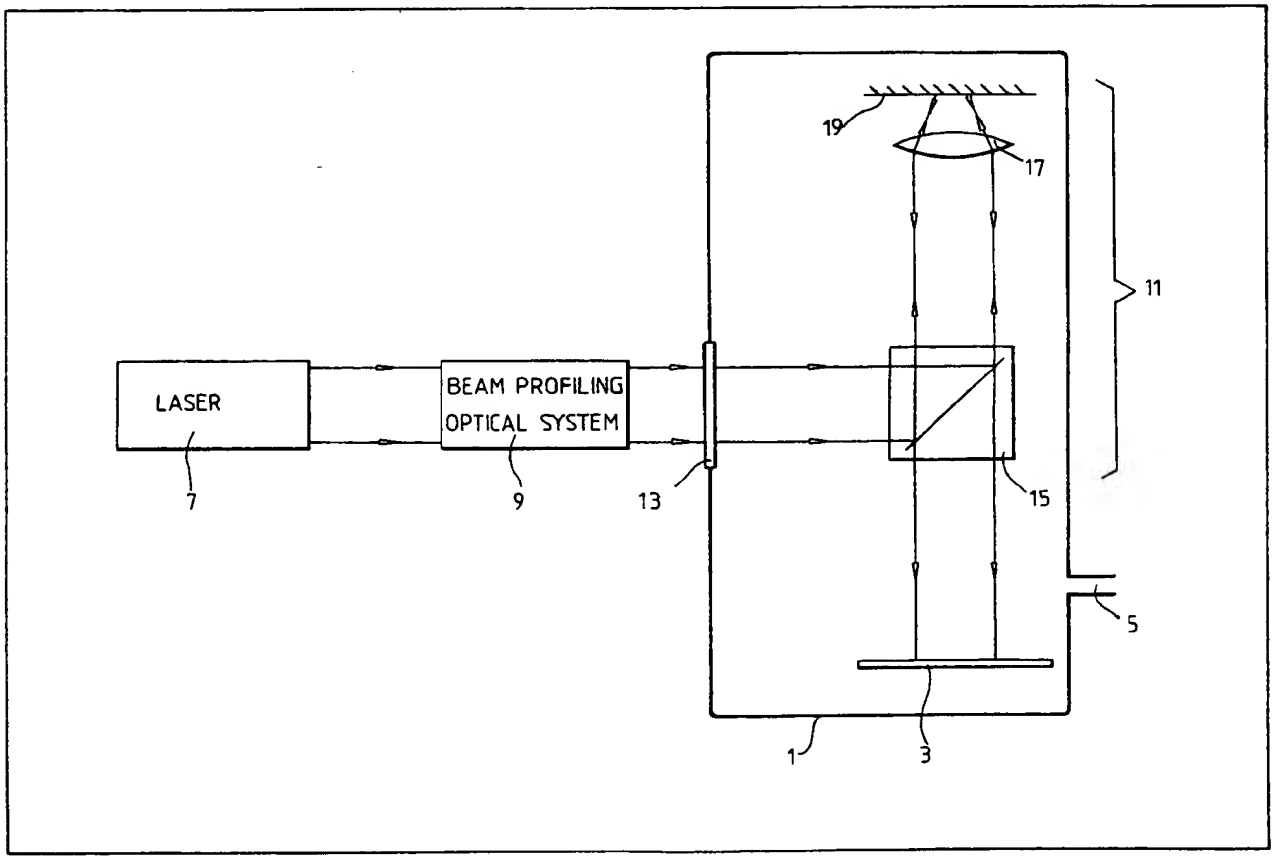
(54) Fabricating semiconductor circuits

(57) A method of annealing (eg. driving in and activating impurities in) selected regions of a semi-conductor substrate 3 during fabrication of a circuit in the substrate. A laser beam is directed onto the substrate 3 through a mask 13 which shields the non-selected regions of the substrate from the laser beam, the masked beam being focussed onto the substrate 3 by an optical system 11.



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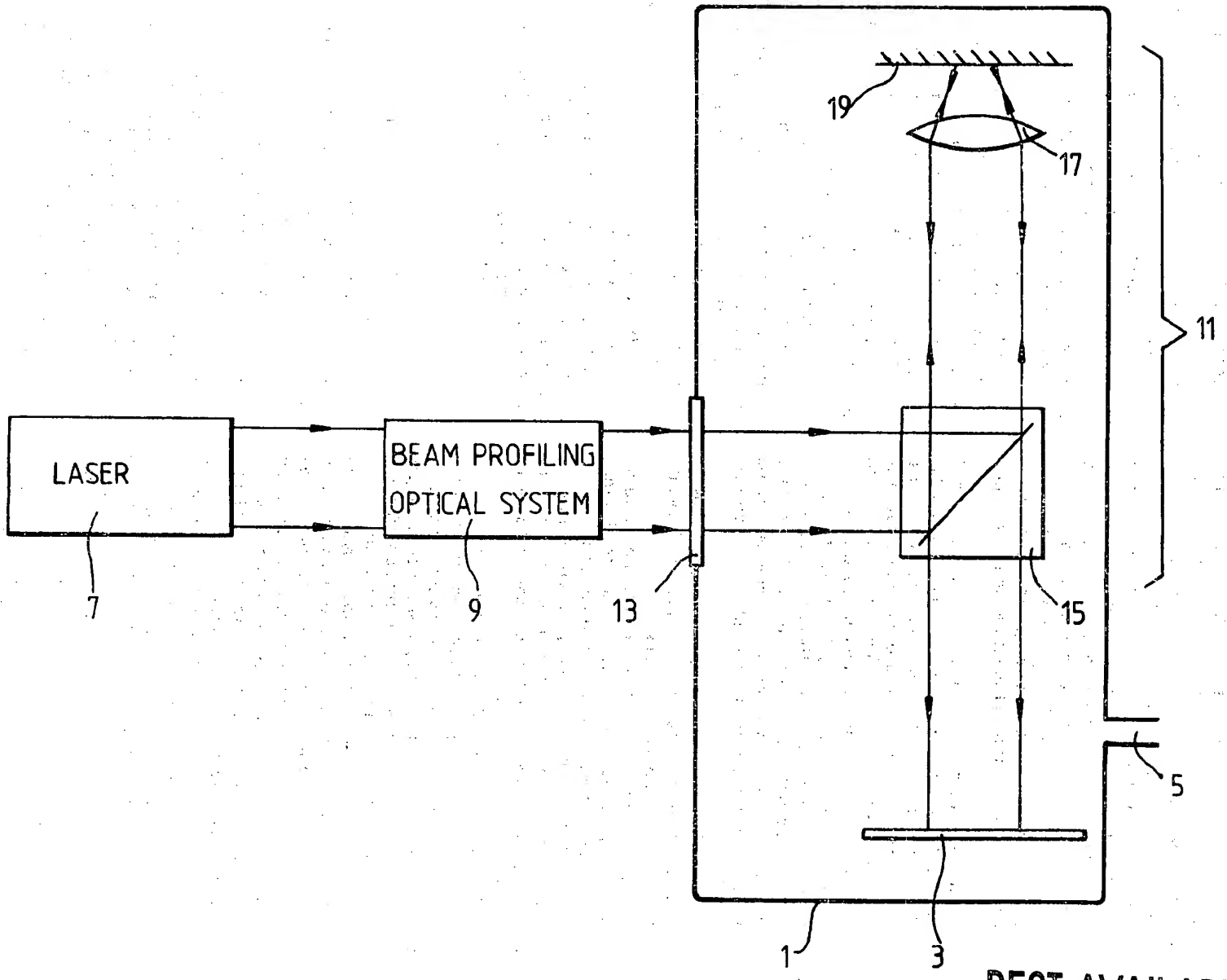

SPECIFICATION

Fabricating semiconductor circuits

This invention relates to methods of fabricating semiconductor circuits.

A basic feature of conventional methods of fabricating semiconductor circuits is the formation, on the surface of a substrate of semiconductor material, of a layer of material in which are formed windows which define selected regions of the substrate into which dopant material is required to be introduced. A series of diffusions or ion-implantations is then used to introduce dopant material through the windows into the regions of the substrate defined by the windows followed by controlled furnace anneals to drive the dopant material into the substrate and cause the doped regions of the substrate to become electrically active.

It has been demonstrated that a beam of laser radiation, either in the form of a pulsed beam illuminating the whole substrate or a scanned cw beam, may be used as an alternative to furnace annealing. However, extreme care must then be taken to avoid damage to the masking layer defining the windows. One proposed method of overcoming this difficulty is to deposit additional layers to reflect radiation away from the substrate except from the doped regions it is desired to anneal. However, this technique requires several preparation steps and is difficult to carry out satisfactorily.

It is an object of the present invention to provide an alternative laser annealing technique which avoids the above mentioned difficulties.

According to the present invention, a method of annealing selected regions of a substrate of semiconductor material during fabrication of a circuit in the substrate comprises directing a beam of radiation onto said substrate through a mask such that non-selected regions are shielded from said radiation by the mask.

The radiation is suitably laser radiation.

The invention also provides an apparatus for carrying out a method according to the invention comprising: a source of radiation; an optical system arranged to direct radiation from said source onto a surface of a semiconductor body; and means for mounting a mask between the source and the optical system; the optical system being adapted to provide an image of the mask on the surface of the semiconductor body.

One method and apparatus in accordance with the invention will now be described, by way of example, with reference to the accompanying drawing which is a schematic diagram of the apparatus.

Referring to the drawing, the apparatus comprises a chamber 1 in which a silicon substrate 3 to be processed is contained, the substrate containing a predefined pattern of doped regions which it is desired to anneal. The atmosphere within the chamber 1 is controllable by means of a vacuum and gas handling system (not shown) connected with the chamber via a suitable duct 5.

Radiation derived from a laser 7, for example a Q-switched ruby laser, is directed onto a main face of the substrate 3 by way of a beam profiling optical system 9 and a further optical system 11. The optical system 11 is disposed in the chamber 1 and a mask 13 is disposed in the wall of the chamber 1 in the path of the radiation between the two optical systems 9 and 11.

The beam profiling system 9 is used to process the spatial intensity of the laser beam so as to produce a beam which is uniform over its cross-section to within a few per cent. The system 9 suitably comprises a lens arrangement or a laser amplifier running in saturation.

The system 11 comprises a high quality beam splitter 15 which deflects the beam received through the mask 13 through a lens system 17 onto a phase conjugate mirror 19, the lens system 17 serving to reduce the size of the projected mask to match the aperture of the mirror 19. After reflection at the mirror 19 the radiation passes through the beam splitter 15 to impinge on the substrate 3 which is positioned at an optically equivalent position to the mask 13.

The mask 13 comprises a metal pattern on a thin quartz plate, the pattern corresponding to areas of the substrate 3 which it is not desired to anneal, i.e. to those areas of the substrate 3 which are required to be shielded from the radiation.

In use of the apparatus the substrate 3 is first accurately positioned with respect to the projected image of the mask 13, and the laser 7 then pulsed at high power to effect the required annealing as rapidly as possible. Alignment of mask image and substrate 3 may be facilitated by incorporating a few alignment holes (not shown) in the mask 13 and aligning the images of the holes with corresponding holes etched in the substrate 3. A low power helium-neon or other suitable laser may be used for this purpose.

To reduce the risk of laser induced damage to the mask 13 and optical systems 9 and 11, the peak power passing through these components may be limited to a suitably low level, and the laser energy raised to the required level for annealing by a laser amplifier (not shown positioned at the optically equivalent position to the mask 13.

CLAIMS

1. A method of annealing selected regions of a substrate of semiconductor material during fabrication of a circuit in the substrate comprising directing a beam of radiation onto said substrate through a mask such that non-selected regions are shielded from said radiation by the mask.

2. A method according to Claim 1 in which said radiation is laser radiation.

3. An apparatus for carrying out a method according to either one of the preceding claims, comprising: a source of radiation; an optical system arranged to direct radiation from said source onto a surface of a semiconductor body; and means for mounting a mask between the source and the optical system, the optical system being adapted to provide an image of the mask on the surface of the semiconductor body.

4. An apparatus according to Claim 3 in which said optical system comprises: a beam splitter arranged to direct radiation after it has passed through said mask onto a phase conjugate mirror

arranged to reflect said radiation through said beam splitter onto said surface.

5. An apparatus according to Claim 4 in which a lens system is interposed in the radiation path between said beam splitter and said mirror, said lens system being effective to substantially match area of said radiation beam to the aperture of said mirror.

6. An apparatus according to Claim 3 or Claim 4 in which a laser amplifier in interposed in the radiation path between said beam splitter and said surface.

7. A method of annealing selected regions of a substrate of semiconductor material during fabrication of a circuit in the substrate, substantially as herinbefore described, with reference to the accompanying drawing.

8. An apparatus for carrying out the method of Claim 7, substantially as hereinbefore described with reference to the accompanying drawings.

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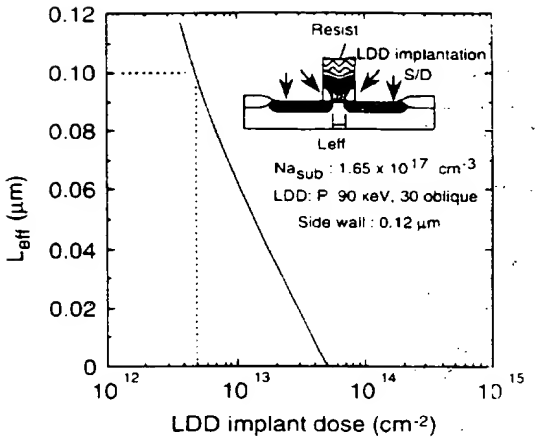
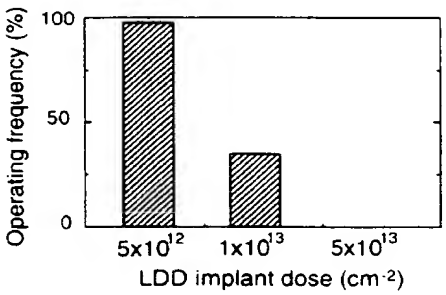


(a) Effective channel length as a function of LDD implant dose



(b) Operating frequencies of 0.1μm gate MOSFETs for LDD implant dose

Fig. 11. Estimated effective channel length for various doses in LDD formation (a) and that for the number of operating sample for 0.1 μm gate MOSFET (b)

sample. This indicates that lateral dopant diffusion is controlled in laser annealing.

3.4. *Effectiveness of oblique ion implantation*

For sub-0.1 μm gate MOSFETs, the LDD formation is an important process because even a little lateral dopant diffusion into the channel may reduce its operational speed. In the present experiment, the effective channel length was defined as the distance between the positions where dopant concentrations in the source and drain are the same as the dopant concentration of channel. We estimate effective channels formed after LDD implantation through side wall spacers. With optimized pulse energy, LA can activate dopants effectively without diffusion, and, consequently, the channel length is determined simply by the as-implanted profile. In other words, the lateral dopant distribution is uniquely controlled by the implantation dose and energy[16]. For n-MOSFET fabrication, phosphorus atoms and boron atoms are used for LDD and channel dopants, respectively. We now estimate the channel lengths for various implant doses, assuming that the adjusting threshold voltage implantation is controlled with a dose of 2×10^{12} cm^{-2} at 15 keV using boron ions. For LDD formation, phosphorus ions were used, since their atomic mass is smaller than that of arsenic, so the implantation damage is expected to be smaller. An oblique angle of 30° to the substrate was chosen normal to avoid ion beam impingement along the base of trenches (which was measured from Fig. 2). The effective channel length (L_{eff}) is estimated based on LSS theory as a function of LDD implantation dose, as shown in Fig. 11(a). L_{eff} decreases as the dose increases. It is difficult to measure the actual channel length because the cross section of the gate is too small. To assess the effectiveness of oblique ion implantation for narrow channel formation using the LA technique, we investigated the relation between the number of operating samples and the estimated effective channel lengths for a 0.1 μm gate MOSFET. The result is shown in Fig. 11(b). The number of operational samples decreases as the effective channel length decreases. The possibility of operational failure may relate to the margin between gate length and effective channel length. This suggests that controlling the effective channel by LDD dose is a useful technique to achieve normal operation of a 0.1 μm MOSFET.

4. CONCLUSION

Sub-0.1 μm gate formation using a space-narrowing technique and laser annealing by SELA in fine MOS device fabrication were studied. Using these techniques, sub-0.1 μm n-MOSFETs were fabricated and their normal operation was confirmed. Oblique ion implantation through side wall spacers was investigated for narrow channel formation. Additionally, the possibility of operational failure and estimated channel length was investigated.

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